CLAIMS

1. A method for rapidly switching between tasks in a microcomputer having a multiplicity of registers that are selectively multiplexed to communicate with a central processing unit (CPU), and a register set memory for storing a multiplicity of register sets and being dual addressed for reading a first register set simultaneously with writing a second register set, each said register set designated for performing a task, said method comprising:

(a) providing a first set of latches and a second set of latches;

(b) writing a first register set, processed by said CPU into said first set of latches in a first clock cycle;

(c) reading a second register set from said register set memory and storing said second register set in said second set of latches in said first clock cycle; and

(d) reading a third register set from said second latch set and storing said third register set into said register set memory, also in said first clock cycle.

2. A method for ordering the performance of tasks in a computer system, said method comprising:

(a) maintaining a priority level for each task;

(b) incrementing each priority level as a function of time; and

(c) beginning the execution of a first task when said priority level of said first task exceeds said priority level of all other tasks.

3. A computer adapted to store a record of executed instructions and comprising:

(a) a memory block having a set of memory block input pins and a set of output pins;

(b) a central processing unit having a set of CPU output pins;

(c) a set of latches, collectively having a set of latch output pins; and

(d) a multiplexor assembly, having at least a first set of input pins and a second set of input pins, a set of multiplexor output pins and a switching pin and wherein said first set of input pins is communicatively connected to said CPU output pins, said second set of input pins is communicatively connected to said latch output pins and said multiplexor output pins are communicatively connected to said memory block input pins, whereby said output of said CPU can be selectively stored in said memory block for future examination.

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